

**DCME-UNI**  
**User Information Manual**



**CLEARPOINT INC.**





**Clearpoint Research Corporation**  
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# **DCME-UNI**

## **USER INFORMATION MANUAL**

All Clearpoint products are exhaustively tested prior to shipment to insure superior field performance. Failures in the field are largely attributed to component failure due to improper handling. Be sure to take all necessary precautions during installation, particularly for grounding to protect against ESD damage (electro-static discharge).

Revision 1.01

**If my memory serves me right . . . It must be Clearpoint.**

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4103-4104  
4105-4106  
4107-4108  
4109-4110  
4111-4112  
4113-4114  
4115-4116  
4117-4118  
4119-4120  
4121-4122  
4123-4124  
4125-4126  
4127-4128  
4129-4130  
4131-4132  
413

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AMERICAN CHEMICAL SOCIETY  
1115 SIXTH AVENUE  
NEW YORK, N.Y. 10020

RE: [illegible]

Enclosed for your information are  
three copies of a manuscript  
entitled [illegible]  
which I am submitting for your  
consideration.

## CHAPTER 1

### DESCRIPTIONS AND SPECIFICATIONS

#### 1.1 THE DCME-UNI

This manual provides user information for the DCME-UNI memory board. The DCME-UNI module supplies high density, low-cost per bit storage for systems utilizing the Digital Equipment Corporation (DEC) UNIBUS. 64 Kb dynamic RAMS are used as individual storage devices, providing up to one megabyte on a single hex-height board. The following list notes the features of the DCME-UNI:

- o Up to one megabyte storage capacity
- o Jumper selectable 18 or 22 bit address
- o Complete hardware/software compatibility with DEC UNIBUS systems
- o An on-board parity control and status register that can be programmed to any one of 16 assigned I/O page addresses
- o Battery Backup Support
- o Single five volt power supply
- o Starting address is programmable at any 32 Kb boundary
- o Parity error LED provides visual indication of board failure



## DESCRIPTIONS AND SPECIFICATIONS

### 1.2 GENERAL DESCRIPTION

The DCME-UNI is a single hex-height memory module which interfaces with the UNIBUS. Provided on board are timing and control logic for the memory, refresh circuitry, and a parity control and status register (CSR).

The MOS memory array consists of up to eight rows of 65,436 x 1 bit dynamic RAM devices, 18 devices per row. Each row consists of 65,436 18 bit words composed of two eight bit bytes and two parity bits, one for each byte. Circuitry to refresh the MOS memory devices is provided on board and operates transparently to the user.

The starting address of the DCME-UNI is selectable using jumpers S1 and S2 (see Figure 1). It can be located at any 32 Kb boundary within the 22- or 18-bit address space of the UNIBUS.

THE DCME-UNI allows the top 4K addresses to be reserved for I/O peripherals.

### 1.3 DCME-UNI SPECIFICATIONS

CHARACTERISTICS	SPECIFICATIONS
Memory device type	MOS dynamic RAM (65,436 x 1)
Access time	290 nsec typical
Memory cycle time	450 nsec typical
Operating temperature	0 to +50 degrees C
Storage temperature	-40 to +85 degrees C
Relative humidity	up to 90% (non-condensing)
Voltages required	+5V +/-5% pins
Battery backup voltage	Factory wired
+5V operating current	2.9 amps
+5V battery backup current	1.5 amps
Refresh	On board
Parity	Incorporates all functions of M7850 parity controller

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2. [Illegible]

3. [Illegible]

4. [Illegible]

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6. [Illegible]

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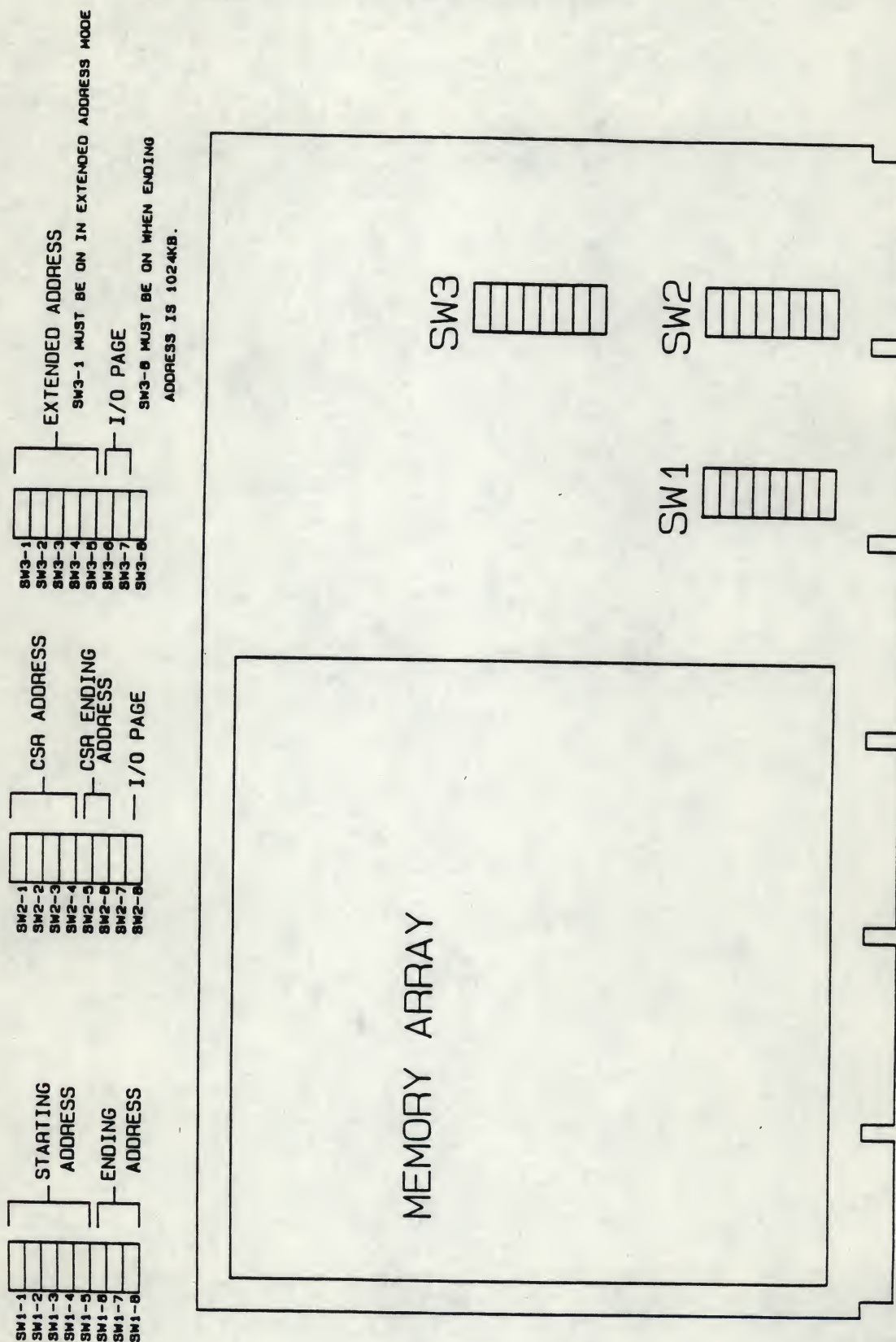
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# DESCRIPTIONS AND SPECIFICATIONS

FIGURE 1  
DCME-UNI JUMPER DESCRIPTION





## DESCRIPTIONS AND SPECIFICATIONS

### 1.4 PARITY CONTROL AND CHECKING

A parity bit is generated for each byte of data written to the DCME-UNI module. The parity bit is stored along with the byte of data in the memory array. Whenever a byte of data is read, it is checked against the stored parity bit. If the parity logic detects an error, the data is assumed to be incorrect.

A parity control and status register (CSR) is provided on the DCME-UNI board. This register is both hardware and software compatible with UNIBUS systems.

The CSR enables the board to generate an interrupt when an error has occurred. It then latches the upper address bits of the locations at which the error occurred; and sets the parity error flag. For diagnostic purposes, the CSR also enables generation of incorrect parity on memory writes. (See Chapter 3 for a detailed description of the CSR.)

### 1.5 BACKPLANE PIN UTILIZATION

The backplane power pins required for the DCME-UNI are outlined in Table 1. The subsequent illustration, Table 2, notes pins used for other signals.

TABLE 1  
BACKPLANE POWER PINS REQUIRED

VOLTAGE -----	PIN ---
+5 NORMAL	AA2, BA2, CA2
GROUND	AC2, AT1, BC2, BT1, CC2, CT1 DC2, DT1, EC2, ET1, FC2, FT1
+5 BATTERY (if used)	BD1

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# DESCRIPTIONS AND SPECIFICATIONS

TABLE 2  
BACKPLANE I/O SIGNAL PINS

SIGNAL -----	PIN ---
A00L	BH2
A01L	BH1
A02L	BJ2
A03L	BJ1
A04L	BK2
A05L	BK1
A06L	BL2
A07L	BL1
A08L	BM2
A09L	BM1
A10L	BN2
A11L	BN1
A12L	BP2
A13L	BP1
A14L	BR2
A15L	BR1
A16L	BS2
A17L	BS1
C0L	BU2
C1L	BT2
A18L	BE2
A19L	BE1
A20L	AP1
A21L	AN1
D00L	AC1
D01L	AD2
D02L	AD1
D03L	AE2
D04L	AE1
D05L	AF2
D06L	AF1
D07L	AH2
D08L	AH1
D09L	AJ2
D10L	AJ1
D11L	AK2
D12L	AK1
D13L	AL2
D14L	AL1
D15L	AM2
INITL	AA1
MYSNL	BV1
PBL	AN2
DCLOL	BF2
SSYNL	BU1



## DESCRIPTIONS AND SPECIFICATIONS

Grant continuity lines are pre-wired at the factory. Table 3 shows where they are located.

TABLE 3  
GRANT CONTINUITY LINES

Bus Grant Lines -----	Finger Pins (Pre-wired at factory) -----
BG4	DS2 to DT2
BG5	DP2 to DR2
BG6	DM2 to DN2
BG7	DK2 to DL2

### NOTE:

Bus grant lines NPGIN to NPGOUT can be configured with optional pins CA1 and CB1.

1947-1948  
1949-1950  
1951-1952

1953-1954  
1955-1956  
1957-1958

1959-1960  
1961-1962  
1963-1964

1965-1966  
1967-1968  
1969-1970

1971-1972  
1973-1974  
1975-1976

1977-1978  
1979-1980  
1981-1982

1983-1984  
1985-1986  
1987-1988

1989-1990  
1991-1992  
1993-1994

1995-1996  
1997-1998  
1999-2000

2001-2002  
2003-2004  
2005-2006

## CHAPTER 2

### HARDWARE INSTALLATION AND INSPECTION

#### 2.1 INTRODUCTION

This chapter provides information for configuring the DCME-UNI jumper options prior to system installation, as well as installation and checkout procedures.

#### 2.2 CONFIGURING DCME-UNI JUMPERS

The locations of the various DCME-UNI option jumpers and an illustration of how to use them are shown in Figure 1 (see Chapter 1). Inspect the module prior to installation to assure that it has been properly configured. Sections 2.3 through 2.5 describe the various DCME-UNI jumper options.

#### 2.3 ADDRESSING OPTIONS

The DCME-UNI addressing logic is set for 22 bit operation. The 22-bit UNIBUS addressing provide access to contiguous bytes from zero to two megawords, utilizing pins AN1, AP1, BE1, and BE2 for the upper four bits of addressing.

The memory starting address may be programmed using S1 to S5 at any 32 Kb boundary, providing up to 1024 Kb.

To configure the starting address, S1-1 through S1-5 must be set accordingly. Table 4 shows the starting address configurations. The ending address must also be programmed on the DCME-UNI module using S1-6, S1-7, S1-8, S2-5, and S2-6. These configurations are charted in Table 5.



# HARDWARE INSTALLATION AND INSPECTION

**TABLE 4**  
**STARTING ADDRESS OPTIONS**

Starting Address	S1-1	S1-2	S1-3	S1-4	S1-5
0 Kb	0	0	0	0	0
32 Kb	0	0	0	0	1
64 Kb	0	0	0	1	0
96 Kb	0	0	0	1	1
128 Kb	0	0	1	0	0
160 Kb	0	0	1	0	1
192 Kb	0	0	1	1	0
224 Kb	0	0	1	1	1
256 Kb	0	1	0	0	0
288 Kb	0	1	0	0	1
320 Kb	0	1	0	1	0
352 Kb	0	1	0	1	1
384 Kb	0	1	1	0	0
416 Kb	0	1	1	0	1
448 Kb	0	1	1	1	0
480 Kb	0	1	1	1	1
512 Kb	1	0	0	0	0
544 Kb	1	0	0	0	1
576 Kb	1	0	0	1	0
608 Kb	1	0	0	1	1
640 Kb	1	0	1	0	0
672 Kb	1	0	1	0	1
704 Kb	1	0	1	1	0
736 Kb	1	0	1	1	1
768 Kb	1	1	0	0	0
800 Kb	1	1	0	0	1
832 Kb	1	1	0	1	0
864 Kb	1	1	0	1	1
896 Kb	1	1	1	0	0
928 Kb	1	1	1	0	1
960 Kb	1	1	1	1	0
992 Kb	1	1	1	1	1

0="OFF" position

1="ON" position



# HARDWARE INSTALLATION AND INSPECTION

TABLE 5  
ENDING ADDRESS OPTIONS

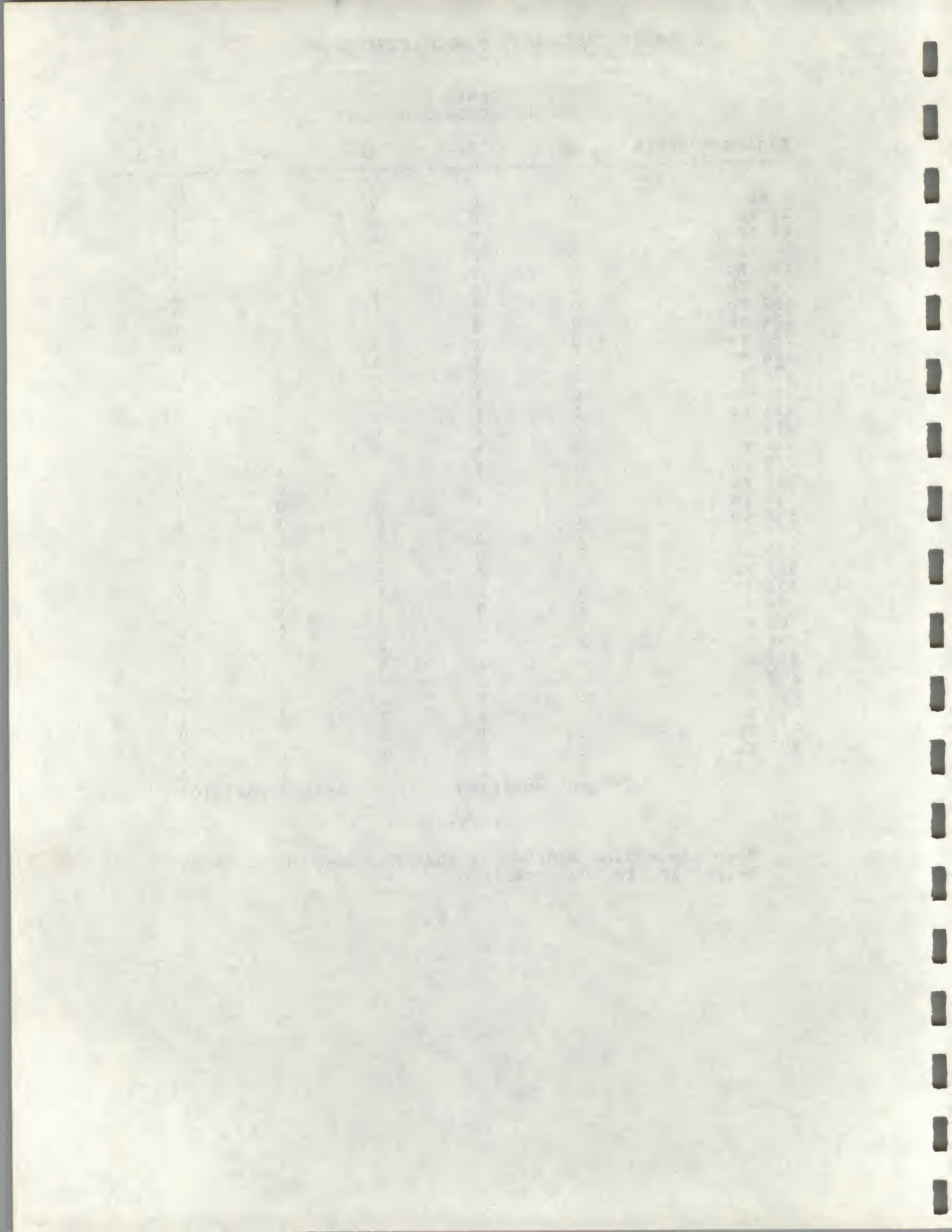
Ending Address	S1-6	S1-7	S1-8	S2-5	S2-6
0 Kb	0	0	0	0	0
32 Kb	0	0	0	0	1
64 Kb	0	0	0	1	0
96 Kb	0	0	0	1	1
128 Kb	0	0	1	0	0
160 Kb	0	0	1	0	1
192 Kb	0	0	1	1	0
224 Kb	0	0	1	1	1
256 Kb	0	1	0	0	0
288 Kb	0	1	0	0	1
320 Kb	0	1	0	1	0
352 Kb	0	1	0	1	1
384 Kb	0	1	1	0	0
416 Kb	0	1	1	0	1
448 Kb	0	1	1	1	0
480 Kb	0	1	1	1	1
512 Kb	1	0	0	0	0
544 Kb	1	0	0	0	1
576 Kb	1	0	0	1	0
608 Kb	1	0	0	1	1
640 Kb	1	0	1	0	0
672 Kb	1	0	1	0	1
704 Kb	1	0	1	1	0
736 Kb	1	0	1	1	1
768 Kb	1	1	0	0	0
800 Kb	1	1	0	0	1
832 Kb	1	1	0	1	0
864 Kb	1	1	0	1	1
896 Kb	1	1	1	0	0
928 Kb	1	1	1	0	1
960 Kb	1	1	1	1	0
992 Kb	1	1	1	1	1
1024 Kb*	1	1	1	1	1

0="OFF" position

1="ON" position

## NOTE:

When the ending address is 1024 Kb, S3-6 must also be set in the "ON" position.



## HARDWARE INSTALLATION AND INSPECTION

The DCME-UNI allows the top 4000 addresses to be reserved for I/O peripherals. More address space may be reserved depending on the number of peripherals in the system. Table 6 shows the configurations for the I/O page jumpers.

**TABLE 6**  
**I/O PAGE JUMPER FUNCTIONS**

I/O PAGE SIZE	S2-8	S3-6	S3-7
Full 1024 Kb	0	1	x
4Kb I/O page	1	0	1
8Kb I/O page	1	0	0
Short Board (Less than 1024 Kb)	0	0	x

0="OFF" position    1="ON" position    x=immaterial

NOTE: SHORT BOARD

These settings are for boards that have less than 1024 Kb capacities and the ending address is not at the maximum boundary.

### 2.4 EXTENDED ADDRESSING OPTION

The DCME-UNI is designed to support 22 bit addressing for paging of up to four 1024 Kb boards in a system. The I/O page is reserved from address 177760000 to address 17777776 in this configuration. The extended addressing option is enabled by using S3-1 through S3-5, depending on which address the DCME-UNI will answer.

NOTE:

Jumper S3-1 must be set "ON" to select each board's unique address of the CSR when in Extended Addressing mode.

The jumper settings are shown in Table 7.

**TABLE 7**  
**EXTENDED ADDRESSING**

Board #	S3-1	S3-2	S3-3	S3-4	S3-5	Memory Bank
0	1	1	0	0	0	000-1024 Kb
1	1	0	1	0	0	1024-2048 Kb
2	1	0	0	1	0	2048-3072 Kb
3	1	0	0	0	1	3072-4096 Kb

0="OFF" position    1="ON" position

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4. A DEPOSIT OF \$1.00 MUST BE MADE

5. A LIBRARY CARD MUST BE OBTAINED

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12. A DEPOSIT OF \$1.00 MUST BE MADE

13. A LIBRARY CARD MUST BE OBTAINED

14. A DEPOSIT OF \$1.00 MUST BE MADE

15. A LIBRARY CARD MUST BE OBTAINED

16. A DEPOSIT OF \$1.00 MUST BE MADE  
17. A LIBRARY CARD MUST BE OBTAINED  
18. A DEPOSIT OF \$1.00 MUST BE MADE

19. A LIBRARY CARD MUST BE OBTAINED

# HARDWARE INSTALLATION AND INSPECTION

## 2.5 18 BIT ADDRESSING MODIFIED INSTALLATION

The DCME-UNI has a 22 bit addressing scheme which utilizes pins AN1, AP1, BE1, and BE2 for the upper four bits of addressing. If the board is used in a backplane where these pins are normally grounded, such as the DD11-P (K) (F), DD11-C, or DD11-D, only 256 Kbs of memory will be accessible. Therefore, the starting and ending addresses must be modified, as shown in Tables 8 and 9. Also, Extended Addressing must be set to board number 3.

**TABLE 8**  
**18 BIT ADDRESSING STARTING ADDRESS**

Starting Address	S1-1	S1-2	S1-3	S1-4	S1-5
0 Kb	1	1	0	0	0
32 Kb	1	1	0	0	1
64 Kb	1	1	0	1	0
96 Kb	1	1	0	1	1
128 Kb	1	1	1	0	0
160 Kb	1	1	1	0	1
192 Kb	1	1	1	1	0
224 Kb	1	1	1	1	1

0="OFF" position

1="ON" position

**TABLE 9**  
**18 BIT ADDRESSING ENDING ADDRESS**

Ending Address	S1-6	S1-7	S1-8	S2-5	S2-6	S2-8	S3-7
0 Kb	1	1	0	0	0	0	x
32 Kb	1	1	0	0	1	0	x
64 Kb	1	1	0	1	0	0	x
96 Kb	1	1	0	1	1	0	x
128 Kb	1	1	1	0	0	0	x
160 Kb	1	1	1	0	1	0	x
192 Kb	1	1	1	1	0	0	x
224 Kb	1	1	1	1	1	0	x
240 Kb							
(8Kb I/O)	1	1	1	1	1	1	0
248 Kb							
(4Kb I/O)	1	1	1	1	1	1	1

0="OFF" position

1="ON" position

x=immaterial

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1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
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1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
---	---	---	---	---	---	---	---	---	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	-----

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## HARDWARE INSTALLATION AND INSPECTION

### 2.6 OPTION JUMPER CONFIGURATIONS

The CSR has an I/O page address in the top 4Kb of memory. This address can be any one of 16 specified locations reserved by DEC for this purpose. The I/O page address may be optionally extended to the top 8K of memory. jumpers S2-1, S2-2, S2-3, and S2-4 are used to select one of the reserved addresses. Table 10 illustrates the use of these jumpers.

#### NOTE:

Each memory board used in a system must be configured to a different address.

TABLE 10  
CSR ADDRESS SELECTION

CSR Address	S2-1	S2-2	S2-3	S2-4
17772100	1	1	1	1
17772102	1	1	1	0
17772104	1	1	0	1
17772106	1	1	0	0
17772110	1	0	1	1
17772112	1	0	1	0
17772114	1	0	0	1
17772116	1	0	0	0
17772120	0	1	1	1
17772122	0	1	1	0
17772124	0	1	0	1
17772126	0	1	0	0
17772130	0	0	1	1
17772132	0	0	1	0
17772134	0	0	0	1
17772136	0	0	0	0

0="OFF" position      1="ON" position

#### NOTE:

In Extended Addressing mode, S3-1 must be set "ON."

### 2.7 BATTERY BACKUP OPTION

The DCME-UNI memory requires 5 volts to retain data. If the 5 V power supply is removed from the board, system memory data is lost.

If battery power is available to maintain system memory data during power failures, the DCME-UNI can be configured to utilize the battery backup option. Battery backup 5 V must be available on backplane pin BD1.



## HARDWARE INSTALLATION AND INSPECTION

For +5 normal voltage, jumper J2 must be installed. To utilize +5 battery backup, J1 must be installed.

### 2.8 INSTALLATION

This is the procedure that should be followed when a CLEARPOINT MEMORY board is received:

1. Visually inspect the module to make sure that it has arrived in good condition.
2. The DCME-UNI is shipped with factory-configured jumpers appropriate for the memory size and location. (A jumper function summary list is included as Appendix A.)
3. Verify that the required power connections (shown in Table 2) are available on the backplane.
4. Jumpers J1 or J2 should be configured on the board to match the power available in the backplane. J1 must be set "ON" if battery backup is to be supplied. If battery backup is not supplied, data will not be retained when AC power is removed.
5. Power down the system. Make sure that the system's power is off before plugging in a module.
6. Plug the board into the UNIBUS. Presently, three backplanes can be used with the DCME-UNI. They are DD11-C, DD11-D, and DD11-P. The DD11-C is a four-slot backplane, and the DCME-UNI can be inserted into slot 2 or slot 3 in this instance. The DD11-P is a nine-slot backplane which is used with the PDP-11/04 or the PDP-11/34. (See Appendix B for further compatible backplane information.)

#### NOTE

Make sure that the module is not being inserted backwards. The component side must face in the same direction as other modules in the system.

7. Power up the system and run the DEC memory MS11 diagnostic program to verify operable memory.

If a problem should arise or for further information, contact Clearpoint Product Support Engineering at 1-800-322-CLPT (2578).

1. The first part of the document is a letter from the President of the United States to the Congress, dated January 3, 1862. It is a very important document, as it contains the President's annual message to Congress. The letter is written in a formal, dignified style, and it is one of the most important documents in the history of the United States.

2. The second part of the document is a report from the Secretary of the Interior, dated January 10, 1862. It is a very important document, as it contains the Secretary's annual report to the President. The report is written in a formal, dignified style, and it is one of the most important documents in the history of the United States.

3. The third part of the document is a report from the Secretary of the Treasury, dated January 15, 1862. It is a very important document, as it contains the Secretary's annual report to the President. The report is written in a formal, dignified style, and it is one of the most important documents in the history of the United States.

4. The fourth part of the document is a report from the Secretary of the War, dated January 20, 1862. It is a very important document, as it contains the Secretary's annual report to the President. The report is written in a formal, dignified style, and it is one of the most important documents in the history of the United States.

5. The fifth part of the document is a report from the Secretary of the Navy, dated January 25, 1862. It is a very important document, as it contains the Secretary's annual report to the President. The report is written in a formal, dignified style, and it is one of the most important documents in the history of the United States.

6. The sixth part of the document is a report from the Secretary of the State, dated January 30, 1862. It is a very important document, as it contains the Secretary's annual report to the President. The report is written in a formal, dignified style, and it is one of the most important documents in the history of the United States.

7. The seventh part of the document is a report from the Secretary of the War, dated February 5, 1862. It is a very important document, as it contains the Secretary's annual report to the President. The report is written in a formal, dignified style, and it is one of the most important documents in the history of the United States.

8. The eighth part of the document is a report from the Secretary of the Navy, dated February 10, 1862. It is a very important document, as it contains the Secretary's annual report to the President. The report is written in a formal, dignified style, and it is one of the most important documents in the history of the United States.

9. The ninth part of the document is a report from the Secretary of the State, dated February 15, 1862. It is a very important document, as it contains the Secretary's annual report to the President. The report is written in a formal, dignified style, and it is one of the most important documents in the history of the United States.

10. The tenth part of the document is a report from the Secretary of the War, dated February 20, 1862. It is a very important document, as it contains the Secretary's annual report to the President. The report is written in a formal, dignified style, and it is one of the most important documents in the history of the United States.

## CHAPTER 3

### CSR DESCRIPTION

#### 3.1 INTRODUCTION

A parity bit is generated for each byte of data written to the DCME-UNI module. The parity bit is stored along with the byte of data in the memory array. Whenever a byte of data is read, it is checked against the stored parity bit. If the parity logic detects an error, the data is assumed to be incorrect.

In order for the software to utilize the parity generation and checking circuitry, a control and status register (CSR) is provided on the DCME-UNI module. It is program compatible with the DEC M7850 parity module.

The CSR is assigned an address in the I/O page (see Table 10 in Chapter 2). The CSR address is programmable to any one of 16 addresses between 772100 and 772136 by jumpers S2-1 through S2-4, as shown in Table 10. The CSR may be accessed by software. When a parity error is detected, the CSR generates an interrupt, latches the upper address bits of the memory location at which the error has occurred, sets the parity error flag, and displays the Board Select line instead of the address error lines. It can be addressed in word mode only.

A unique CSR address must be selected for each board. The user should not use addresses already employed by the system.

#### NOTE:

When using Extended Addressing mode, jumper S3-1 must be set in the "ON" position.

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## CSR DESCRIPTION

### 3.2 CSR BIT ASSIGNMENT

The CSR is a 16 bit register located in the I/O page. The following list describes the functions of each one of the 16 bits:

Bit 0 - Parity Error Interrupt Enable

If set to 1, the memory board will interrupt the processor on error, and generate BUS parity line to read the memory location at which there is a parity error. This bit is read- and write-enabled.

Bit 1 - UNUSED

Bit 2 - Write Wrong Parity

If this bit is set to 1, any word or byte written to the array will be stored along with an incorrect parity bit. This is for maintenance purposes. It enables diagnostics to test the board's ability to detect errors and interrupt when enabled.

Bit 3 - UNUSED

Bit 4 - UNUSED

Bits 5-11 - Latch Address Bits

When a parity error is detected, the upper address bits of the failing location are latched. These bits are read- and write-enabled and will contain data from the BUS, the upper address bits containing parity error, or the Board Select address if a parity error has occurred.

Bit 12 - UNUSED

Bit 13 - UNUSED

Bit 14 - Extended CSR Read Enable

This bit is a read- and write-enabled bit that is used to control the data to be loaded into CSR Bits 5 through 11. If Bit 14 set to 0, then CSR Bits 5 through 11 will contain either the data written into the register, or the address Bits 11-17 if a parity error has occurred. If Bit 14 is set to 1 and a parity error has occurred, CSR Bits 5 through 8 will contain Board Select 0 through Board Select 3 at the time of the last parity error.

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## CSR DESCRIPTION

### Bit 15 - Parity Error Flag

This bit is read- and write-enabled. It is used to indicate a memory parity error, or one that was forced by writing into this bit. A parity error has occurred when it is a logical one.

### TRADEMARKS:

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APPENDIX A  
JUMPER FUNCTION SUMMARY LIST

Jumpers	Function
S1-1 through S1-5	DCME-UNI starting address
S1-6 through S1-8 S2-5 through S2-6	DCME-UNI ending address
S2-1 through S2-4	CSR register address select
S2-7	Disable CSR
S2-8	I/O page select
S3-1	Enable extended CSR
S3-2 through S3-5	Board enable
S3-6	Full 1024 Kb board (No I/O page)
S3-7	4K or 8K I/O select
S3-8	Disable CSR Bit 14

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APPENDIX B  
COMPATIBLE BACKPLANES

Backplanes DD11-C, DD11-P (K) (F), and DD11-D can be used with the DCME-UNI in DEC computer models 11/04 to 11/60 without modification.

Backplane MF11-U can be used with some modifications. They are as follows:

- o Pin 2BU2 wire wrapped to 2BU1
- o Pin LBF2 wire wrapped to 2BF2
- o Pins 2AS1 and 2AR1 must be isolated from ground
- o Pin 2AS1 wire wrapped to 3AK1
- o Pin 2AR1 wire wrapped to 3AA1
- o SS-11 may not be jumpered for battery backup
- o SS-11 board may be plugged into the parity model slot 2

The DCME-UNI may also be used in backplanes MF11-L (P), ME11-L, and DD11-B with the following modifications:

- o Pin AR1 must be isolated from ground and wire wrapped to CU1
- o Pin AS1 must be isolated from ground and wire wrapped to CB2
- o SS-11 may not be jumpered for battery backup

CONSTITUTIONAL HISTORY

The history of the constitution of the United States is a subject of great interest and importance. It is a subject which has attracted the attention of the people of this country for many years.

The constitution of the United States is a document which has been the subject of much discussion and debate. It is a document which has been the subject of much discussion and debate.

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